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Modelling of the film thickness effecton the carrier's mobility in polysilicon thin film transistors

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Abstract

The transfer characteristics modelisation of the Mosfet's structure allows us to simulate the doping effect, the grains size, the layer thickness as well as others parameters of the transistor. The purpose of this work is to study the effect of the layer thickness on the carriers's mobility in the channel.For that, a two-dimensional modelling of the electrical conduction in amorphous silicon Mosfet's is used. It is based on the solving of Poisson's equation and the two continuity current equations of electrons and holes, and takes into account of the properties of polysilicon material, such as a density of trapped states formed by two exponential band tails, and gaussian state distribution for the dangling bonds. The grain boundary is modelised as a nearly amorphous semiconductor, having a finite width, providing an additional scattering or a barrier for the charge carriers. The numerical model assumes a drift- diffusion mechanism in the crystalline regions in series with a thermionic emission mechanism for carriers overcoming the grain boundary potential barrier. In order to validate the conduction model, we also incorporate the effect of the electrical field on the generation carriers at grain boundary traps. The transfer characteristics are studied in function of film thickness, then the carrier's mobility. The results show that, the surface field affects only the low thicknesses, the variation of this field as a function of film thickness is sufficient to explain the behaviour of channel mobility. For high thicknesses, the field effect mobility is controlled by intergranular barriers of potential.

Keywords: Thin -Film Transistor, Field Effect Mobility, Dangling Bonds, and Band tails.

1. Introduction

Polycrystalline silicon is a promising candidate for the fabrication of thin-film transistors used to control the pixel voltage of active- matrix liquid –crystal displays [1]. Most authors adopt a so called "diffusion model", where current transport across the grain boundary is not considered [2]-[3]. In this paper, we have developed a numerical method to simulate I_{DS} (V_{GS}) characteristics of amorphous silicon Mosfets in which current transport across the grain boundary is taken into account by using thermionic emission current in series with drift-diffusion current in the bulk. The numerical solution of the system of equations allows us to analyze, versus film thickness, the transfer characteristics then the field effect mobility calcu-

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lated in accumulation regime. We first describe the physical and numerical model used in this study, next we present our simulated results which are discussed.

2. The studied structure

Fig 1 shows a schematic cross section of accumulation-mode MOSFET structure. The starting material for device fabrication was silicon wafers. A 100nm SiO_2 layer was thermally grown on RCA cleaned substrates. Amorphous silicon thin films were deposited using low pressure chemical vapour deposition (LPVCD) technique, then recrystallized at 600°C, and doped with a dose of 6e12cm^{-2} (1e17cm^{-3}) to produce a channel layer . Source and drain were formed by 3e20cm^{-3} boron implantation, and are assumed to extend in the whole thickness of polycrystalline layer. The gate oxide was grown to a thickness of 100nm.

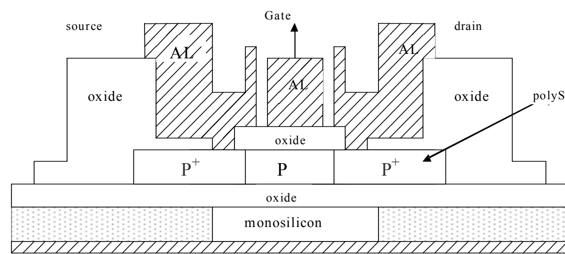

Fig 1: Polycrystalline silicon thin film transistor structure used in this study.

3. Geometrical and physical model

Fig (2) gives the geometrical model for the transistor. In this computation, the polysilicon material is assumed to be composed of a succession of crystallites, having a grain size of L_L nm and of L_T nm in respectively, lateral and transverse direction.. L_T is variable as a function of layer thickness. We also assume that the impurity atoms are totally ionized. Traps are supposed to be uniformly distributed at grain boundaries which are assumed as parallel and perpendicular to the interfaces Si/SiO_2.

The standard density of states model of amorphous silicon is used to describe the gap states distribution in amorphous grain boundaries. As shown in fig (3), it consists on:

Two exponential distributions of valence-band tail (VBT) and conduction-band tail (CBT) states, characterized respectively by their total density g_{Dmax}, g_{Amax} and their characteristic energies of the acceptor-like KT_A and the donor-like KT_D.

and Gaussian distributions for the dangling bonds (DB), symmetrically located with reference to the mid gap, and characterized by the total density N_{DB}, the standard deviation σ_{DB}, and the positive correlation energy ΔEd.

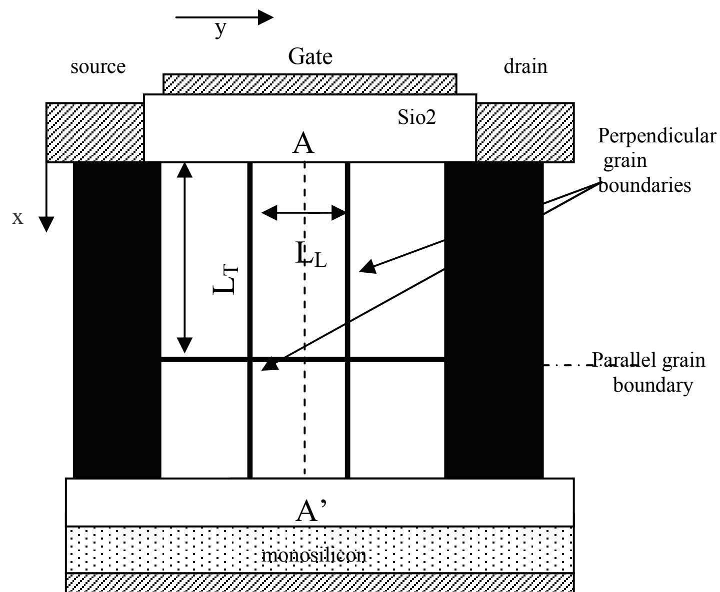

Fig2: Geometrical model for the studied structure.

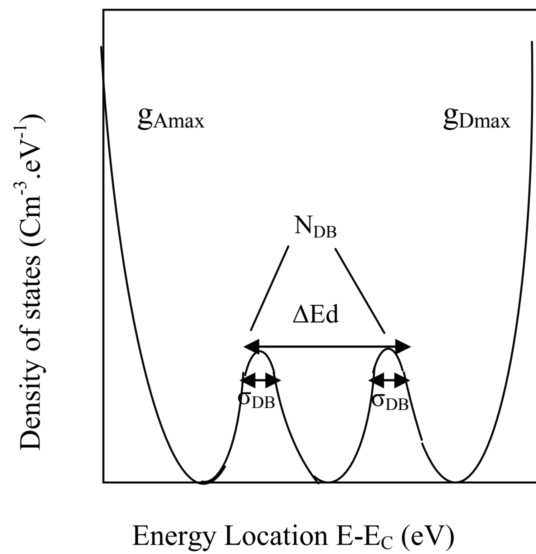

Fig3: Schematic representation of polysilicon gap state profile considered in the simulation.

4. Numerical model

A detailed analysis of polysilicon thin film transistors requires the simultaneous and numerical solution of equations, which describe the steady state conduction phenomena inside semiconductor devices. Set of used equations consists on:

$$\begin{cases} Div\left(\varepsilon\,\overrightarrow{grad\varphi}\right) = -q\left(p - n + dop + \sum N_T\right) \\ 1/q\,div\left(\overrightarrow{Jn}\right) = U \\ 1/q\,div\left(\overrightarrow{J_P}\right) = -U \end{cases} \quad (1)$$

In the bulk of crystallites, conduction currents are given by:

$$\overrightarrow{J_n} = -q\left(n\mu_n\,\overrightarrow{grad\varphi_n}\right) \quad (2)$$

$$\overrightarrow{J_p} = -q\left(p\mu_p\,\overrightarrow{grad\varphi_p}\right) \quad (3)$$

In the following, we describe how the current across the grain boundary is treated in the present model. As an example, the continuity equation for electrons is considered.
Using mesh numbers and the corresponding variables shown in fig(4), discretized continuity equations for electrons can be written respectively as:

$$(J_n(i,m) - J_n(i,m-1))/\Delta x_{m-1} = qU_{i,j} \quad (4)$$

and

$$(J_n(i,m+1) - J_n(i,m))/\Delta x_m = qU_{i,j+1} \quad (5)$$

for mesh (i, j) and for mesh (i,j+1), respectively. In these equations, $J_n(i,m-1)$ and $J_n(i,m+1)$ can be formulated using equation (2). However, $J_n(i,m)$ represents the electron current across the grain boundary and cannot be expressed in a form similar to equation (2). Therefore, another treatment for it is necessary.

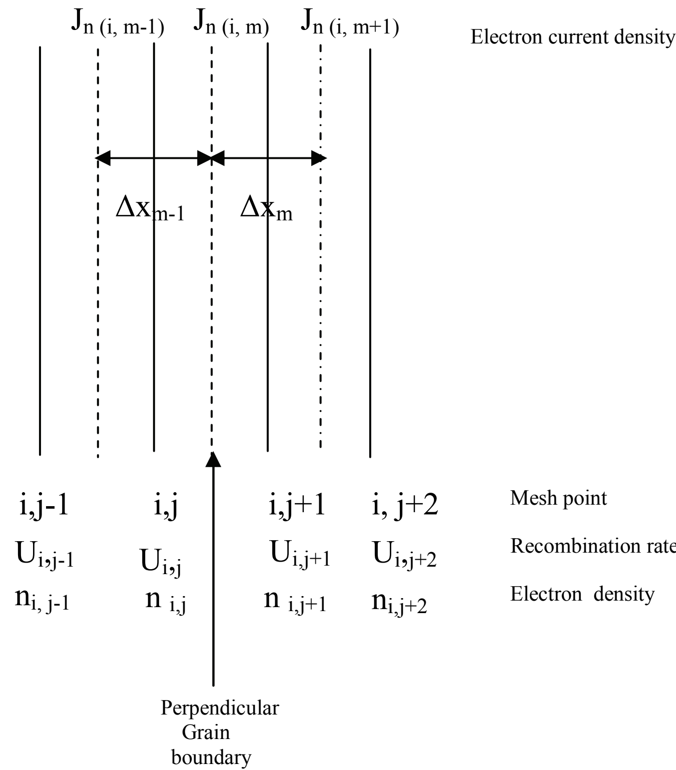

Fig 4: Mesh spacing and variables around a perpendicular grain boundary.

Hence, in the present model, we give an expression for $J_n(i,m)$ in (4) and (5) by considering a current transport mechanism across the grain boundary. We formulate it by using the thermionic emission current.

Indeed, being modeled as a nearly amorphous semiconductor, with energy band gap of 1.5-1.6eV [4], the grain boundary potential barrier turns out to be ≈ egb/2= 0.75-0.80eV and becomes comparable to that observed in the depletion region which can attain Eg/2= 0.56eV for the studied doping level. In this case, this mechanism becomes important and should be considered. But only in the direction of the current flow (at perpendicular grain boundaries).It can be expressed for electrons as:

$$\overrightarrow{J_n(i,m)} = -q\Pi_n V_n \left(n_{i,j} - n_{i,j+1}\right) \quad (6)$$

The continuity equations for holes are treated similarly, by replacing equations (4), (5) and (6) respectively by:

$$(J_p(i,m) - J_p(i,m-1)) / \Delta x_{m-1} = qU_{i,j} \quad (7)$$

$$(J_p(i,m+1) - J_p(i,m)) / \Delta x_m = qU_{i,j+1} \quad (8)$$

$$\overrightarrow{J_p(i,m)} = -q\Pi_p V_p \left(p_{i,j} - p_{i,j+1}\right) \quad (9)$$

In these equations, used symbols are
ε the permittivity of the material,
n(p) the free electrons(holes) density,
φ, φ_n, φ_p the electrostatic potential, the electron and hole electrochemical Fermi potentials respectively,
μ_n , μ_p the electron and hole mobilities respectively,
Dop the net doping of the channel,
U the net active generation-recombinaison rate,
$\sum N_T$ the sum of the different trap centers present in the material.
Π_n , Π_p the transmissions factors for electrons and holes.
V_n , V_p the thermal speeds of electrons and holes respectively
n_{ij} , $n_{i,j+1}$, p_{ij} , $p_{i,j+1}$ are respectively, the free electrons and holes density at both sides of the grain boundary.

Because the nonlinearity of the three coupled partial equations of the system (1).The determination of unknown variables values requires a numerical method of differential equation resolution We have used the method called “finite difference” [5]. The obtained linear system is then solved by Gauss method.

5. Results of simulation and discussions

The physical and technological parameters used in the calculation procedure to simulate I_{DS}= f(V_{GS}) characteristics of the Mosfet structure are reported in table 1.
Fig (5) shows the simulated transfer characteristics of the TFT. The drain current I_{DS} is plotted as a function of the gate voltage V_{GS} , for different values of film thickness. V_{DS} being fixed to – 0,5V, when a parallel grain boundary is located at 60nm from the lower interface.
The numerically calculated device characteristics closely resemble those shown experimentally [6]. On the one hand, one notices, that the currents increase with the film thickness. This can be explained by the decrease of the polycrystalline layer resistance. On the other hand, and in depletion regime, the rate of increase of the current decreases when the layer thickness increases. Indeed, the behaviour of this current as a function of film thickness and gate voltage can be explained by the simultaneous variation of the average electric field in the structure and of the extension of the emission zone, as reported by Greve and al [7]. Also, these curves show the existence of four distinct zones:

1- In accumulation regime, we can observe a first zone (zone1) where the current increases rapidly according to the gate voltage and a second zone (zone2) which corresponds to “on state” of the transistor.
2- In depletion regime, “off state”, the behavior of the structure is different. It is characterized by the leakage current I_L coming from: the ohmic conduction of polycrystalline layer between source and drain contacts (zone3) ; and the generation current which is field assisted [8] (zone4). Its variation as a function of gate voltage is related to a POOLE –FRENKEL effect [9].

Parameters	Values
Electron band mobility	700 cm^2/Vs
Hole band mobility	200cm^2/Vs
Oxide thickness	100nm
Polysilicon thickness	Variable
Grain size	200nm
Band tails	
g_{Amax} g_{Dmax} KT_A KT_D C_ntb, C_Ptb	1e20cm^{-3} 1e20cm^{-3} 0.03eV 0.04eV 1e-15 cm^{-2}
Dangling bonds	
N_{DB} σ_{DB} ΔE_d C_ndb, C_Pdb	1e19cm^{-3} 0.05eV 0.2eV 1e-15cm^{-2}
Bandgap energy	1.12eV
Polysilicon doping	1E17cm^{-3}

Table1: Physical and technological parameters used in simulation.

In addition, the large threshold voltage observed in accumulation – mode transistors can only justified by assuming the existence of both acceptor and donor states at grain boundaries. This conclusion is consistent with the generally agreed result that grain boundaries basically behave as majority- carrier traps.

The current increase observed experimentally at positive gate voltage [10], is justified by our numerical model so far implemented, in which the effect of the electrical field on the generation carriers at grain boundary traps is incorporated. Generation currents based on pure thermal emission being very limited and do not appreciably contribute to the leakage current.

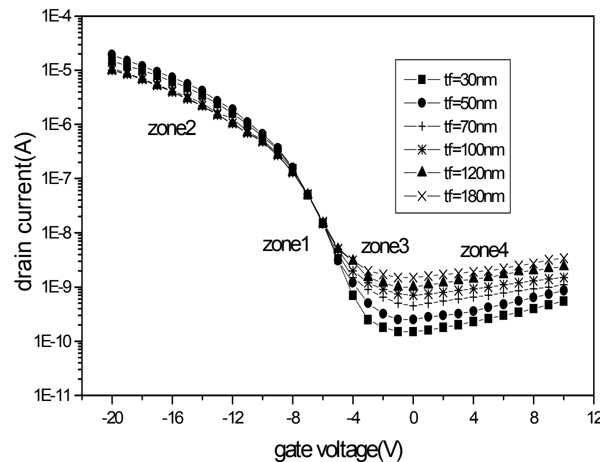

Fig 5: Effect of the film thickness on the $I_{DS}=f(V_{GS})$ simulated characteristics.

6. Study of field effect Mobility

6.1 General aspect

In accumulation regime, this mobility is calculated from the following equation:

$$\mu_{FE} = \frac{\delta I_{DS}}{\delta V_{GS}} \frac{l}{W C_{ox} V_{DS}} \tag{10}$$

W, l, C_{ox}, represent respectively, the width, the length of the channel and the gate capacitance per unit area. Fig (6) shows the variation of this mobility versus layer thickness for various values of the gatevoltage.

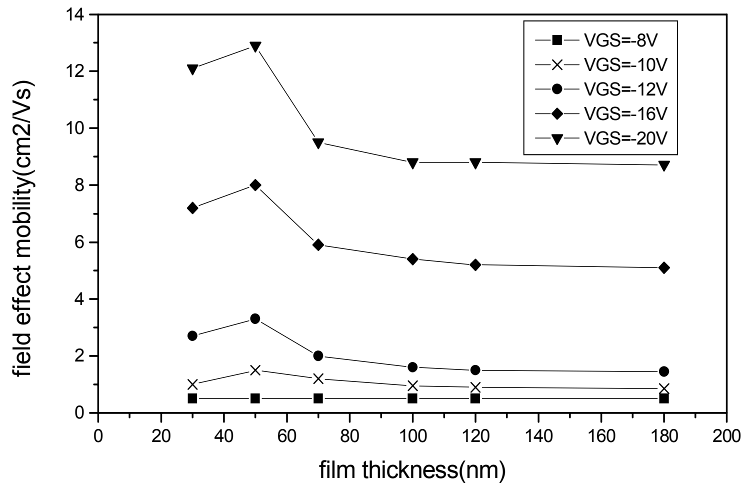

Fig 6: Field effect mobility versus film thickness at different gate voltages.

One notices, on the one hand, that this one increases with the gate voltage V_{GS}. This can be attributed to the decrease of the potential energy barriers, thereby increasing the number of free carriers in the channel.

On the other hand, for film thickness lower than 70nm, this mobility increases and reaches a maximum. Then it decreases. The fall of the carrier's mobility becomes considerable at high bias voltages.

6.2 Case of low thicknesses

We can notice that the high value of the field effect mobility μ_{FE} depends on the gate voltage V_{GS}. As already mentioned, a peak of mobility is observed for thicknesses inferior to 70 nm, when one increases the gate voltage. Under these conditions, the influence on the mobility of the quality of the interface and of the intensity of the electric field become as significant as that of the intergranular barriers of potential.

This phenomenon was also observed experimentally by Hayashi and al [11], on thin film transistors, in which the polysilicon layers are deposited by LPCVD technique and etched by thermal oxidations at 1000°C.

Based on the previous remarks and in order to understand the role of the gate bias voltages in the manifestation of the phenomenon, we study the distribution of the electric field

in the layer for low thicknesses (only one layer), and for the thicknesses higher than 100 nm constituted by two layers of grain separated by one grain boundary.

For that, we consider the same geometrical model shown in fig (2) and locate the parallel grain boundary at 70nm from the lower interface. The doping, V_{GS}, V_{DS} and L_L are respectively fixed to 1E17cm^{-3},
-10V, -0.5V, and 200 nm.
Fig (7) and Fig (8) show the calculated electric field along the symmetry axis AA', for various layer thicknesses, respectively:
1 - In the absence of the parallel grain boundary for low thicknesses.
2 - In the presence of this grain boundary for high layer thicknesses.
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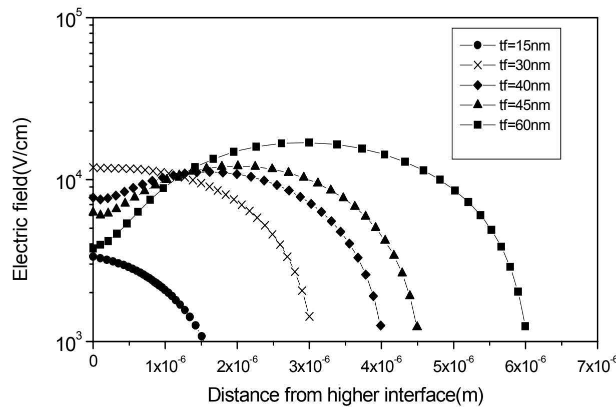

Fig 7: Electrical field along AA' at different thicknesses of the active layer in the absence of the parallel grain boundary.

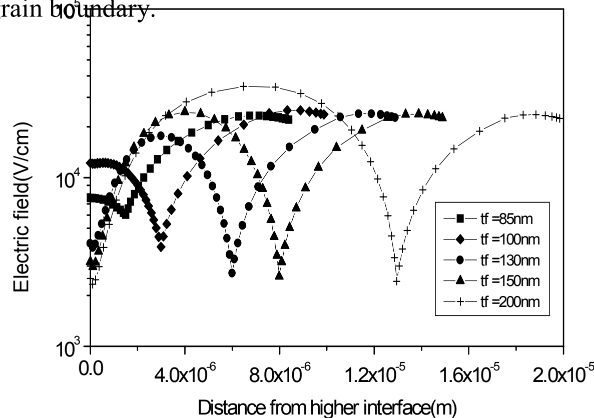

Fig 8: Electrical field along AA' at different thicknesses of the active layer in the presence of the parallel grain boundary.

The simulation demonstrated that the intensity of the field is not uniform in all the layer thickness, and that at the higher interface (A), it depends on the film thickness in the case of low thicknesses or, on the existence and on the position of the parallel grain boundary for high thicknesses, The variation of the surface field versus film thickness is formally related to a coupling phenomenon between the two interfaces (case of low thicknesses), or between the high interface and the parallel grain boundary in the case of high thicknesses.

However, it is the field at the proximity of this interface which influences the mobility of the carriers in the channel. Thus we calculate the intensity of the surface field as a function

of film thickness, for two grain sizes in order to focus our discussion on the sensitivity of this field and hence of the carrier's mobility to this parameter.

I. Effect of Lateral grain size

To put in evidence the effect of lateral grain size in the behaviour of the electric field as a function of film thickness, we calculate the surface field (at the interface A), for two values of this parameter fixed respectively to 100nm and 200nm with the same position of the parallel grain boundary and the same values as previously for V_{GS}, V_{DS} and L_L.

As shown in fig (9), the obtained curves are similar but shifted: the extrema of the curves correspond respectively to different thicknesses.

In addition, we can notice that for any value of the layer thickness, the surface field decreases when the grain size increases. The observed decrease of the field for thickness higher than 100nm, is due to the progressive decoupling of the interface and the parallel grain boundary.

The simulation confirms the fact that the surface field depends on grain sizes. This conclusion is in a good agreement with the experimental results of Balestra and al [12] which have demonstrated that the coupling phenomenon determines the distribution of the electrostatic potential, and that the intensity of this coupling depends on the layer doping, layer thickness, grain sizes, bias gate, and on the density of interface states.

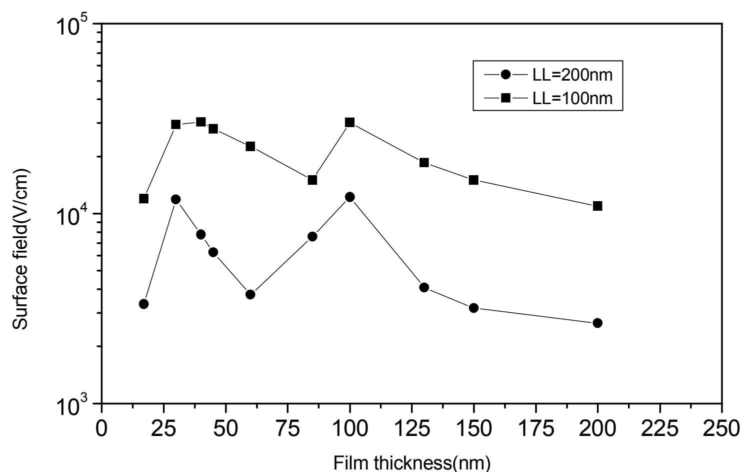

Fig 9: Surface field versus film thickness for two grain sizes.

II- Correlation between the variation of the field and that of mobility

If it is admitted that, by increasing the field in the channel, the carrier's mobility decreases in this one, the results of simulation are in agreement with those of **NOGUCHI** [13] which confirms that:

The field effect mobility is higher for the thinnest films,

For the same thickness, it is also higher when the grain size is larger.

The previous analysis put in evidence, the effect of the electric field on the carrier's mobility in the range of low thicknesses, and the relation existent between the intensity of the surface field, the presence and the position of the parallel grain boundary.

Consequently it permits us, in the range of low thicknesses, to adjust the variation of this field versus film thickness to that of the field effect mobility, while considering the paral-

lel grain boundary located at 60nm from lower interface, with V_{GS}, V_{DS}, L_L fixed respectively to -10V, -0.5V,200nm .

Fig (10) represents, for thickness layer lower than 100nm, the simultaneous variation of the electric field and the carrier's mobility. We can notice clearly that the increase of the surface electric field E_s induces the reduction of the mobility μ_{FE} and the opposite effect is true: the variation of the field is thus sufficient to explain the behaviour of mobility as a function of film thickness..

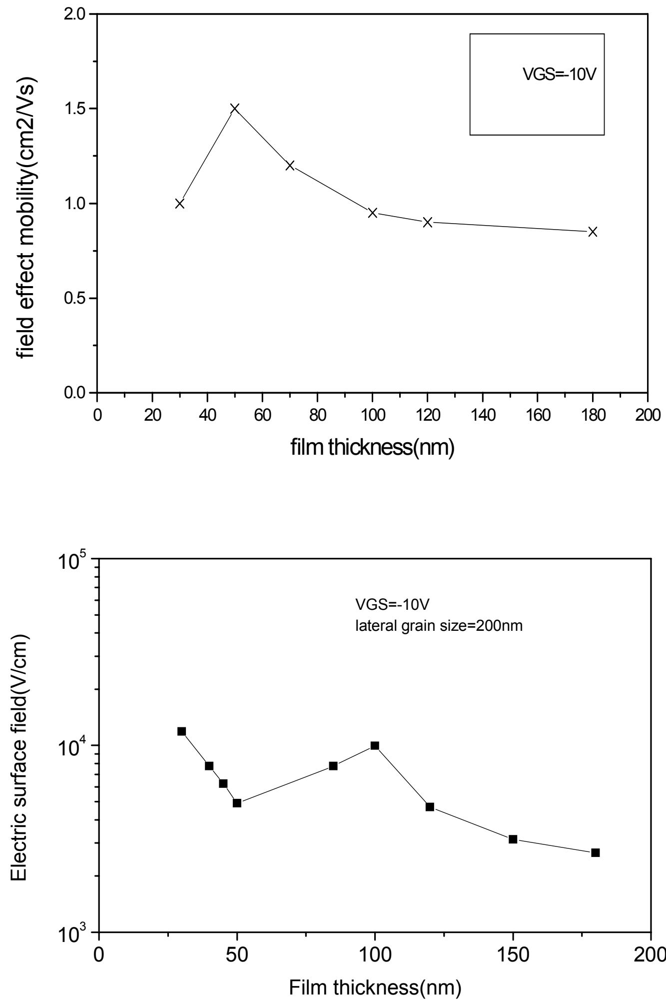

Fig 10: correlation between the effect field mobility and the surface electrical field for low thicknesses

6.3 Case of high thicknesses

The behaviour is different for the layer thicknesses higher than 100nm, for which the field decreases when the thickness increases, until losing its role of “reducer” of mobility: this decrease of the field corresponds to the progressive decoupling of the interface and the parallel grain boundary. The field effect mobility in this case is controlled by the intergranular barriers of potential and not by the surface field. The density of traps being constant in amorphous silicon layers [14], so the carrier’s mobility in the channel does not vary in this range.

7. Conclusion

A numerical model is presented in which thermionic emission is considered at the perpendicular grain boundaries, in series with drift- diffusion in the bulk. This model is more natural than the conventional “diffusion model” in the treatment of current continuity across the grain boundary in polysilicon layers.

The geometrical model considers that a polysilicon layer is constituted by a succession of crystallites.The grain boundaries are parallel and perpendicular to the polysilicon-oxide interfaces. The traps are supposed uniformly distributed at each grain boundary. In this study, we have considered only the effect of film thickness. Others Parameters (doping, density of interfaces states.) will make the object for other eventual studies.

The transfer characteristics show the existence of four zones of conduction and permit us to calculate the field effect mobility.

The electrostatic coupling is a fundamental phenomenon for the interpretation of the evolution of the carrier’s mobility versus layer thickness.

The study evidences, in the range of low thicknesses, the reducing effect of the surface electric field on this one and the existence of a relation between the intensity of the field, the presence, and the position of the parallel grain boundary in the case of high thicknesses, for which the behaviour of carrier’s mobility versus layer thickness is related to barriers of potential.

The simulation was used for determining many parameters of thin film transistors. It inform us about the thickness to choose in order to optimize the performances of polysilicon MOS transistors. Another granular aspect of the active layer will make the object of a future study

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